

### Single-Lane PCIe Equalizer/Redriver

#### **General Description**

The MAX14950A dual equalizer/redriver improves PCI Express® (PCIe) signal integrity by providing programmable input equalization. This feature reduces deterministic jitter and redrives circuitry to reestablish deemphasis, which compensates for circuit-board loss at high frequencies. The device permits optimal placement of key PCIe components and allows for longer runs of stripline, microstrip, or cable.

The device contains two identical channels capable of equalizing PCIe Gen III (8GT/s), Gen II (5GT/s), and Gen I (2.5GT/s) signals and features electrical idle and receiver detection.

The MAX14950A is available in a small, 40-pin, 5.0mm x 5.0mm TQFN package with flow-through traces for optimal layout and minimal space requirements. It is specified over the 0°C to +70°C commercial operating temperature range.

#### **Applications**

Servers

Industrial PCs

Test Equipment

Computers

**External Graphics Applications** 

Communications Switchers

Storage Area Networks

#### **Benefits and Features**

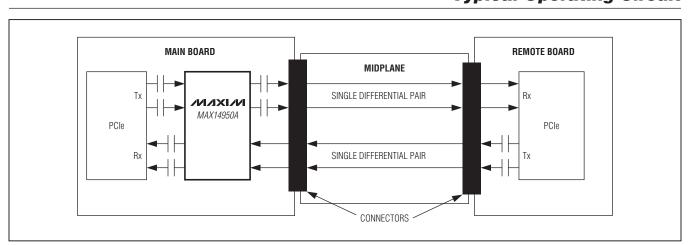
- ♦ Innovative Design Eliminates Need for Costly **External Components**
- ♦ Increased Design Flexibility for Backward-**Compatible Applications** 
  - ♦ Optimized for PCIe Gen III (8GT/s) and Gen II (5GT/s) Signals and Compatible with Gen I (2.5GT/s) Signals
- ♦ High Level of Integration for Performance
  - ♦ Very Low Latency With 160ps (typ) Propagation Delay
  - ♦ PCle Gen III (8GT/s)-Compliant Input/Output **Return Loss**
  - ♦ Four-Level-Programmable Input Equalization
  - **♦ Eight-Level-Programmable Output Emphasis**

  - ♦ Receiver Detection Permits Completely **Transparent Operation**
- ♦ Ideal for Space-Sensitive Applications
  - $\diamond$  On-Chip 50 $\Omega$  Input/Output Terminations
  - ♦ 40-Pin, 5.0mm x 5.0mm TQFN Packaging

Ordering Information appears at end of data sheet.

For related parts and recommended products to use with this part, refer to www.maxim-ic.com/MAX14950A.related.

### **Typical Operating Circuit**



PCI Express is a registered service mark of PCI-SIG Corporation.

MIXIM

Maxim Integrated Products 1

#### **ABSOLUTE MAXIMUM RATINGS**

(Voltages referenced to GND.)	Continuous Power Dissipation (T <sub>A</sub> = +70°C)
V <sub>CC</sub> 0.3V to +4.0V	TQFN (derate 35.7mW/°C above +70°C)2857mW
All Other Pins (Note 1)0.3V to (V <sub>CC</sub> + 0.3V)	Operating Temperature Range
Continuous Current IN_P, IN_M,	Junction Temperature Range40°C to +150°C
OUT_P, OUT_M ±30mA	Storage Temperature Range65°C to +150°C
Peak Current IN_P, IN_M, OUT_P, OUT_M	Lead Temperature (soldering, 10s)+300°C
(pulsed for 1µs, 1% duty cycle)±100mA	Soldering Temperature (reflow)+260°C

Note 1: All I/O pins are clamped by internal diodes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### PACKAGE THERMAL CHARACTERISTICS (Note 2)

Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ )....... 28°C/W Junction-to-Case Thermal Resistance ( $\theta_{JC}$ )......2°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a fourlayer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

#### **ELECTRICAL CHARACTERISTICS**

 $(V_{CC} = +3.0 \text{V to } +3.6 \text{V}, C_{CL} = 200 \text{nF coupling capacitor on each output}, R_L = 50 \Omega$  on each output,  $T_A = 0 ^{\circ}\text{C}$  to  $+70 ^{\circ}\text{C}$ , unless otherwise the coupling capacitor on each output,  $T_A = 0 ^{\circ}\text{C}$  to  $+70 ^{\circ}\text{C}$ , unless otherwise the coupling capacitor on each output,  $T_A = 0 ^{\circ}\text{C}$  to  $+70 ^{\circ}\text{C}$ , unless otherwise the coupling capacitor on each output,  $T_A = 0 ^{\circ}\text{C}$  to  $+70 ^{\circ}\text{C}$ ,  $T_A = 0 ^{\circ}\text{C}$  to  $+70 ^{\circ}\text{C}$ . erwise noted. Typical values are at  $V_{CC} = +3.3V$  and  $T_A = +25$ °C.) (Note 3)

PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE	·						
Power-Supply Range	V <sub>CC</sub>			3.0	3.3	3.6	V
Supply Current			OEQ_2 = OEQ_1 = OEQ_0 = GND		102	135	
			OEQ_2 = OEQ_1 = GND, OEQ_0 = V <sub>CC</sub>		106	140	
		EN = V <sub>CC</sub>	OEQ_2 = OEQ_0 = GND, OEQ_1 = V <sub>CC</sub>		107	140	
			OEQ_2 = GND, OEQ_1 = OEQ_0 = V <sub>CC</sub>		125	160	, no A
	lcc		OEQ_2 = V <sub>CC</sub> , OEQ_1 = OEQ_0 = GND		106	140	- mA
			$OEQ_2 = OEQ_0 = V_{CC}$ , $OEQ_1 = GND$		132	170	
			$OEQ_2 = OEQ_1 = V_{CC}$ , $OEQ_0 = GND$		140	180	
			OEQ_2 = OEQ_1 = OEQ_0 = V <sub>CC</sub>		165	210	

## **Single-Lane PCIe Equalizer/Redriver**

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC}=+3.0V\ to\ +3.6V,\ C_{CL}=200nF\ coupling\ capacitor\ on\ each\ output,\ R_L=50\Omega\ on\ each\ output,\ T_A=0^{\circ}C\ to\ +70^{\circ}C,\ unless\ otherwise\ noted.$  Typical values are at  $V_{CC}=+3.3V\ and\ T_A=+25^{\circ}C.)$  (Note 3)

PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
			OEQ_2 = OEQ_1 = OEQ_0 = GND		57	80	_
			OEQ_2 = OEQ_1 = GND, OEQ_0 = V <sub>CC</sub>		61	85	
			OEQ_2 = OEQ_0 = GND, OEQ_1 = V <sub>CC</sub>		62	85	
Standby Current	lozpy	EN = GND	OEQ_2 = GND, OEQ_1 = OEQ_0 = V <sub>CC</sub>		75	100	mA
Standby Current	ISTBY	EN = GIND	OEQ_2 = V <sub>CC</sub> , OEQ_1 = OEQ_0 = GND		62	80	IIIA
			$OEQ_2 = OEQ_0 = V_{CC},$ $OEQ_1 = GND$		85	110	
			$OEQ_2 = OEQ_1 = V_{CC},$ $OEQ_0 = GND$		92	120	
			OEQ_2 = OEQ_1 = OEQ_0 = V <sub>CC</sub>		120	150	
Differential Input Impedance	Z <sub>RX-DIFF</sub> - DC	DC		80	100	120	Ω
Differential Output Impedance	Z <sub>TX-DIFF-</sub> DC	DC		80	100	120	Ω
Common-Mode Resistance to GND, Input Termination Not Powered	Z <sub>RX-HIGH-</sub>	-150mV ≤ V <sub>II</sub>	N_CM ≤ +200mV	50			kΩ
Common-Mode Resistance to GND, Input Termination Powered	Z <sub>RX-DC</sub>			20	25	30	Ω
Output Short-Circuit Current	I <sub>TX-SHORT</sub>	Single-ended (Note 4)				90	mA
Common-Mode Delta, Between Active and Idle States	VTX-CM- DC-ACTIVE- IDLE-DELTA					100	mV
DC Output Offset, During Active State	V <sub>TX</sub> - ACTIVE- DIFF-DC	I(V <sub>OUT_P</sub> - V <sub>OUT_M</sub> )I				50	mV
DC Output Offset, During Electrical Idle	V <sub>TX-IDLE-</sub> DIFF-DC	I(V <sub>OUT_P</sub> - V	OUT_M)I			50	mV

## **Single-Lane PCIe Equalizer/Redriver**

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC}=+3.0V\ to\ +3.6V,\ C_{CL}=200nF\ coupling\ capacitor\ on\ each\ output,\ R_L=50\Omega\ on\ each\ output,\ T_A=0^{\circ}C\ to\ +70^{\circ}C,\ unless\ otherwise\ noted.$  Typical values are at  $V_{CC}=+3.3V\ and\ T_A=+25^{\circ}C.)$  (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE (Note 4)	•		•			•
		f = 0.05GHz to 1.25GHz	10			dB
Input Return Loss, Differential	RL <sub>RX-DIFF</sub>	f = 1.25GHz to 2.5GHz	8			dB
		f = 2.5GHz to 4GHz	5			dB
Input Return Loss, Common	DI	f = 0.05GHz to 2.5GHz	6			dB
Mode	RL <sub>RX-CM</sub>	f = 2.5GHz to 4GHz	4			dB
		f = 0.05GHz to 1.25GHz	10			dB
Output Return Loss, Differential	RL <sub>TX-DIFF</sub>	f = 1.25GHz to 2.5GHz	8			dB
		f = 2.5GHz to 4GHz	4			dB
Output Return Loss, Common	D.	f = 0.05GHz to 2.5GHz	6			dB
Mode	RL <sub>TX-CM</sub>	f = 2.5GHz to 4GHz	4			dB
Redriver-Operation Differential Input-Signal Range	V <sub>RX-DIFF</sub> -		100		1200	mV <sub>P-P</sub>
Full-Swing Differential Output Voltage (No Deemphasis)	V <sub>TX-DIFF</sub> -	2 x I(V <sub>OUT_P</sub> - V <sub>OUT_M</sub> )I, OEQ_2 = OEQ_1 = OEQ_0 = GND	800	1000	1300	mV <sub>P-P</sub>
Output Deemphasis Ratio, 0dB	V <sub>TX-DE-</sub> RATIO-0dB	OEQ_2 = OEQ_1 = OEQ_0 = GND, Figure 1		0		dB
Output Deemphasis Ratio, 3.5dB	V <sub>TX-DE-</sub> RATIO- 3.5dB	OEQ_2 = OEQ_1 = GND, OEQ_0 = V <sub>CC</sub> , Figure 1		3.5		dB
Output Deemphasis Ratio, 6dB	V <sub>TX-DE-</sub> RATIO-6dB	OEQ_2 = OEQ_0 = GND, OEQ_1 = V <sub>CC</sub> , Figure 1		6		dB
Output Deemphasis Ratio, 6dB with Higher Amplitude	V <sub>TX-DE-HA-</sub> RATIO-6dB	OEQ_2 = GND, OEQ_1 = OEQ_0 = V <sub>CC</sub> , Figure 1		6		dB
Output Deemphasis Ratio, 3.5dB with Preshoot	V <sub>TX-DE-</sub> PS-RATIO- 3.5dB	OEQ_2 = V <sub>CC</sub> , OEQ_1 = OEQ_0 = GND, Figure 1		3.5		dB
Output Deemphasis Ratio, 6dB with Preshoot	V <sub>TX-DE-PS-</sub> RATIO-6dB	OEQ_2 = OEQ_0 = V <sub>CC</sub> , OEQ_1 = GND, Figure 1		6		dB
Output Deemphasis Ratio, 9dB with Preshoot	V <sub>TX-DE-PS-</sub> RATIO-9dB	OEQ_2 = OEQ_1 = V <sub>CC</sub> , OEQ_0 = GND, Figure 1		9		dB
Output Deemphasis Ratio, 9dB with Preshoot and Higher Amplitude	V <sub>TX-DE-PS-</sub> HA-RATIO- 9dB	OEQ_2 = OEQ_1 = OEQ_0 = V <sub>CC</sub> , Figure 1		9		dB
Input Equalization, 3dB	V <sub>RX-EQ-</sub> 3dB	INEQ_1 = INEQ_0 = GND (Note 5)		3		dB

## **Single-Lane PCIe Equalizer/Redriver**

#### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC}=+3.0V\ to\ +3.6V,\ C_{CL}=200nF\ coupling\ capacitor\ on\ each\ output,\ R_L=50\Omega\ on\ each\ output,\ T_A=0^{\circ}C\ to\ +70^{\circ}C,\ unless\ otherwise\ noted.$  Typical values are at  $V_{CC}=+3.3V\ and\ T_A=+25^{\circ}C.)$  (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Equalization, 5dB	V <sub>RX-EQ-</sub> 5dB	INEQ_1 = GND, INEQ_0 = V <sub>CC</sub> (Note	5)		5		dB
Input Equalization, 7dB	V <sub>RX-EQ-</sub> 7dB	INEQ_1 = V <sub>CC</sub> , INEQ_0 = GND (Note 5)			7		dB
Input Equalization, 9dB	V <sub>RX-EQ-</sub> 9dB	INEQ_1 = INEQ_0 = V <sub>CC</sub> (Note 5)			9		dB
Output Common-Mode Voltage	V <sub>TX-CM-</sub> AC-PP	$\begin{array}{c} \text{MAX}(\text{V}_{\text{OUT\_P}} + \text{V}_{\text{OUT\_M}}) / 2 - \text{MIN}(\text{V}_{\text{OU}} \\ \text{V}_{\text{OUT\_M}}) / 2 \end{array}$	T_P +			100	mV <sub>P-P</sub>
Propagation Delay	t <sub>PD</sub>			120	160	240	ps
Rise/Fall Time	t <sub>TX-RISE-</sub> FALL	(Note 6)		20			ps
Rise/Fall Time Mismatch	t <sub>TX-RF-</sub> MISMATCH	(Note 6)				3	ps
Output Skew Same Pair	t <sub>SK</sub>					5	ps
Deterministic Jitter	t <sub>TX-DJ-DD</sub>	K28.5 pattern, AC-coupled, $R_L = 50\Omega$ , deemphasis, no preshoot, data rate = $800$			10.5	23.5	ps <sub>P-P</sub>
Random Jitter	t <sub>TX-RJ-DD</sub>	D10.2 pattern, no deemphasis, no preshoot, data rate = 8GT/s				1.5	ps <sub>RMS</sub>
Electrical Idle Entry Delay	t <sub>TX-IDLE-</sub> SET-TO- IDLE	From input to output, D10.2 pattern, data rate = 1GT/s			5		ns
Electrical Idle Exit Delay	t <sub>TX-IDLE-</sub> TO-DIFF- DATA	From input to output, D10.2 pattern, data rate = 1GT/s			5		ns
		EIL_L = EIH_H = EIH_L = GND		65		175	
		EIL_L = EIH_L = GND, EIH_H = V <sub>CC</sub>		85		215	]
		EIL_L = EIH_H = GND, EIH_L = V <sub>CC</sub>		25		155	
Electrical Idle Detect Threshold (Note 7)	V <sub>TX-IDLE-</sub>		V <sub>IH</sub>	50		175	mV <sub>P-P</sub>
(Note 1)	THRESH	EIL_L = V <sub>CC</sub> , EIH_H = EIH_L = GND	V <sub>IL</sub>	20		165	
			V <sub>IH</sub>	80		205	1
	$EIL\_L = EIH\_H = V_{CC}, EIH\_L = GND                                  $		50		195		
Output Voltage During Electrical Idle (AC)	V <sub>TX-IDLE-</sub> DIFF-AC-P	I(V <sub>OUT_P</sub> - V <sub>OUT_M</sub> )I				20	mV <sub>P-P</sub>
Receiver-Detect Pulse Amplitude	V <sub>TX-RCV-</sub> DETECT	Voltage change in positive direction				600	mV
Receiver-Detect Pulse Width					100		ns
Receiver-Detect Retry Period					200		ns

#### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC}=+3.0V \text{ to } +3.6V, C_{CL}=200 \text{nF} \text{ coupling capacitor on each output, } R_L=50\Omega \text{ on each output, } T_A=0^{\circ}\text{C} \text{ to } +70^{\circ}\text{C}, \text{ unless otherwise noted.}$  Typical values are at  $V_{CC}=+3.3V \text{ and } T_A=+25^{\circ}\text{C.})$  (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL LOGIC						
Input-Logic Level Low	V <sub>IL</sub>				0.6	V
Input-Logic Level High	V <sub>IH</sub>		1.4			V
Input-Logic Hysteresis	V <sub>HYST</sub>			0.1		V
Input Pulldown Resistance	R <sub>PD</sub>		200	375		kΩ
ESD PROTECTION						
ESD Voltage		Human Body Model (HBM)		±4		kV

- Note 3: All devices are 100% production tested at  $T_A = +70$ °C. Specifications over operating temperature range are guaranteed by design.
- Note 4: Guaranteed by design, unless otherwise noted.
- Note 5: Equivalent to same amount of deemphasis driving the input.
- Note 6: Rise and fall times are measured using 20% and 80% levels.
- **Note 7:** Electrical idle detect threshold is measured using D10.2 pattern and data rate = 1GT/s.

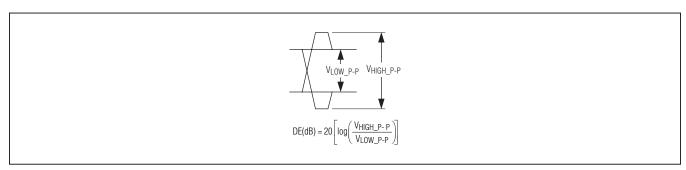
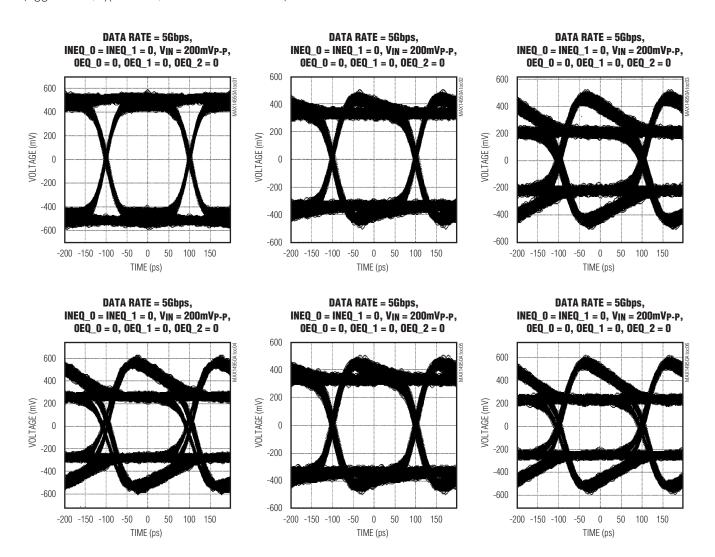


Figure 1. Illustration of Output Deemphasis

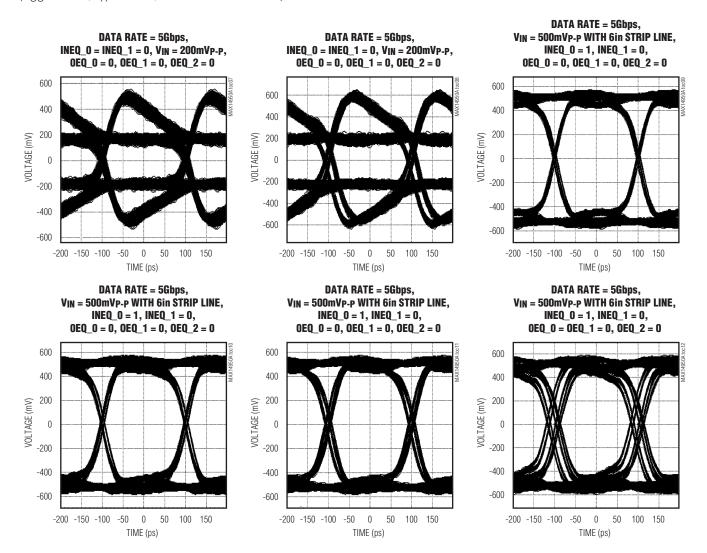
### Single-Lane PCIe Equalizer/Redriver

#### **Typical Operating Characteristics**



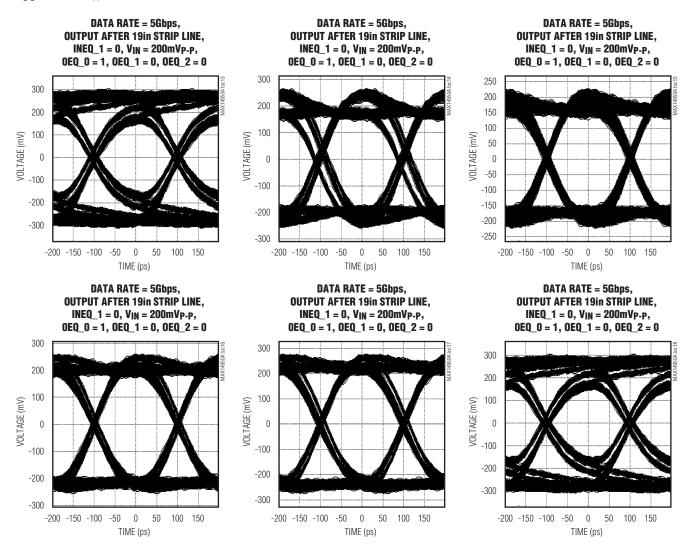
## Single-Lane PCIe Equalizer/Redriver

#### Typical Operating Characteristics (continued)



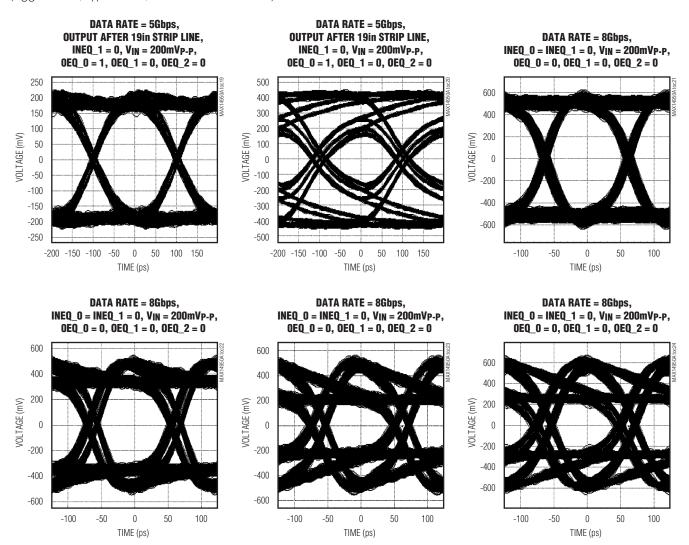
### Single-Lane PCIe Equalizer/Redriver

#### Typical Operating Characteristics (continued)



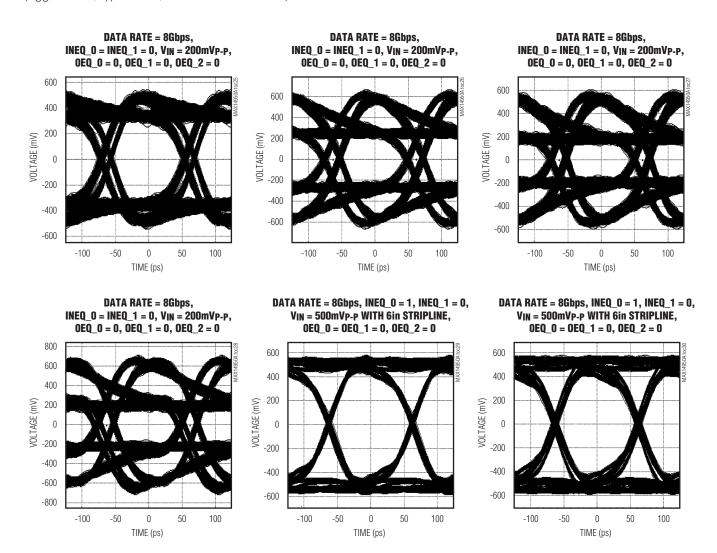
## Single-Lane PCIe Equalizer/Redriver

#### Typical Operating Characteristics (continued)



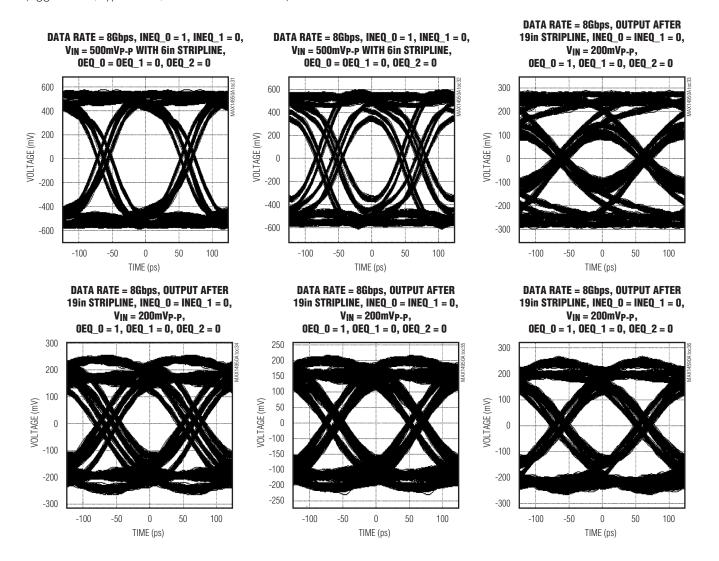
## Single-Lane PCIe Equalizer/Redriver

#### Typical Operating Characteristics (continued)



## Single-Lane PCIe Equalizer/Redriver

#### Typical Operating Characteristics (continued)

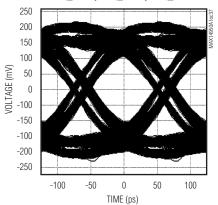


## Single-Lane PCIe Equalizer/Redriver

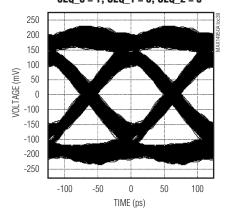
#### **Typical Operating Characteristics (continued)**

 $(V_{CC} = +3.3V, T_A = +25^{\circ}C, unless otherwise noted.)$ 

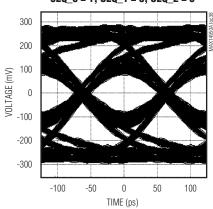




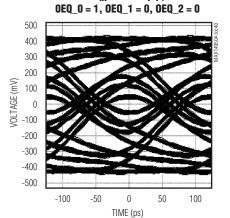
DATA RATE = 8Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ\_0 = INEQ\_1 = 0, V<sub>IN</sub> = 200mV<sub>P-P</sub>,  $0EQ_0 = 1, 0EQ_1 = 0, 0EQ_2 = 0$ 



#### DATA RATE = 8Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ\_0 = INEQ\_1 = 0, $V_{IN} = 200 \text{mV}_{P-P}$ $0EQ_0 = 1, 0EQ_1 = 0, 0EQ_2 = 0$

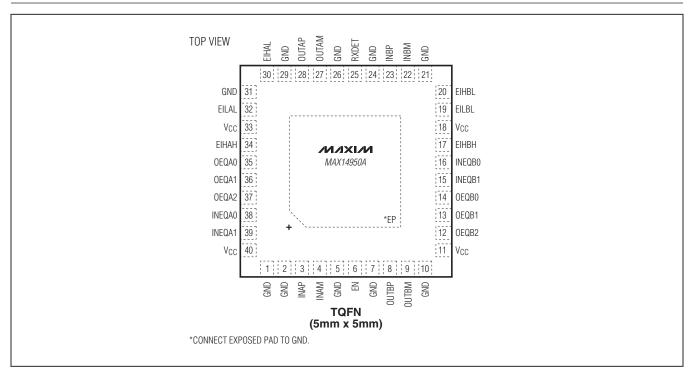


DATA RATE = 8Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ\_0 = INEQ\_1 = 0, V<sub>IN</sub> = 200mV<sub>P-P</sub>,



## **Single-Lane PCIe Equalizer/Redriver**

### **Pin Configuration**



### **Pin Description**

PIN	NAME	FUNCTION
1, 2, 5, 7, 10, 21, 24, 26, 29, 31	GND	Ground
3	INAP	Noninverting Input, Channel A
4	INAM	Inverting Input, Channel A
6	EN	Enable Input. Drive EN low for standby mode. Drive EN high for normal mode. EN has a $375 \text{k}\Omega$ (typ) internal pulldown resistor.
8	OUTBP	Noninverting Output, Channel B
9	OUTBM	Inverting Output, Channel B
11, 18, 33, 40	$V_{CC}$	Power-Supply Input. Bypass $V_{CC}$ to GND with $0.1\mu F$ and $0.01\mu F$ capacitors in parallel as close as possible to the device.
12	OEQB2	Output Deemphasis Control MSB, Channel B. OEQB2 has a 375kΩ (typ) internal pulldown resistor.
13	OEQB1	Output Deemphasis Bit 1, Channel B. OEQB1 has a 375kΩ (typ) internal pulldown resistor.
14	OEQB0	Output Deemphasis Control LSB, Channel B. OEQB0 has a 375kΩ (typ) internal pulldown resistor.
15	INEQB1	Input Equalization Control MSB, Channel B. INEQB1 has a 375kΩ (typ) internal pulldown resistor.
16	INEQB0	Input Equalization Control LSB, Channel B. INEQB0 has a $375 k\Omega$ (typ) internal pulldown resistor.

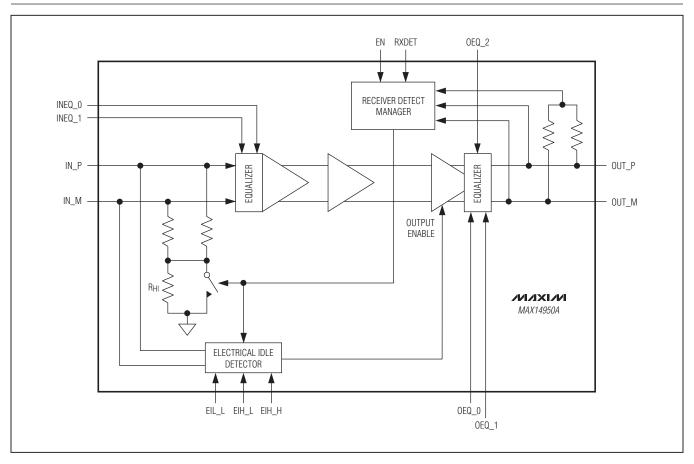
# **Single-Lane PCIe Equalizer/Redriver**

### Pin Description (continued)

PIN	NAME	FUNCTION
17	EIHBH	Electrical Idle High Threshold Increase Control Bit, Channel B. EIHBH has a $375 k\Omega$ (typ) internal pulldown resistor.
19	EILBL	Electrical Idle Low Threshold Decrease Control Bit, Channel B. EILBL has a $375 k\Omega$ (typ) internal pulldown resistor.
20	EIHBL	Electrical Idle High Threshold Decrease Control Bit, Channel B. EIHBL has a $375 \text{k}\Omega$ (typ) internal pulldown resistor.
22	INBM	Inverting Input, Channel B
23	INBP	Noninverting Input, Channel B
25	RXDET	Receiver Detection Control Bit. Toggle RXDET to initiate receiver detection. RXDET has a $375k\Omega$ (typ) internal pulldown resistor.
27	OUTAM	Inverting Output, Channel A
28	OUTAP	Noninverting Output, Channel A
30	EIHAL	Electrical Idle High Threshold Decrease Control Bit, Channel A. EIHAL has a $375 \text{k}\Omega$ (typ) internal pulldown resistor.
32	EILAL	Electrical Idle Low Threshold Decrease Control Bit, Channel A. EILAL has a $375 k\Omega$ (typ) internal pulldown resistor.
34	EIHAH	Electrical Idle High Threshold Increase Control Bit, Channel A. EIHAH has a $375 k\Omega$ (typ) internal pulldown resistor.
35	OEQA0	Output Deemphasis Control LSB, Channel A. OEQA0 has a 375kΩ (typ) internal pulldown resistor.
36	OEQA1	Output Deemphasis Control Bit 1, Channel A. OEQA1 has a 375kΩ (typ) internal pulldown resistor.
37	OEQA2	Output Deemphasis Control MSB, Channel A. OEQA2 has a 375kΩ (typ) internal pulldown resistor.
38	INEQA0	Input Equalization Control LSB, Channel A. INEQA0 has a 375kΩ (typ) internal pulldown resistor.
39	INEQA1	Input Equalization Control MSB, Channel A. INEQA1 has a 375kΩ (typ) internal pulldown resistor.
_	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance and ground conductivity to the device. Do not use EP as the only GND connection.

## **Single-Lane PCIe Equalizer/Redriver**

#### **Functional Diagram**



### **Detailed Description**

The MAX14950A dual equalizer/redriver supports Gen III (8GT/s), Gen II (5GT/s), and Gen I (2.5GT/s) PCIe data rates. The device contains two identical drivers with idle/receive detect on each lane and equalization/ deemphasis/preshoot to compensate for circuit board loss. Programmable input equalization circuitry reduces deterministic jitter, improving signal integrity. The device features programmable output deemphasis/preshoot, permitting optimal placement of key PCIe components and longer runs of stripline, microstrip, or cable.

#### **Programmable Input Equalization**

Programmable input equalization for channel A is controlled by two bits: INEQA1 and INEQA0 and for channel B is controlled by two bits: INEQB1 and INEQB0 (Table 1.)

**Table 1. Input Equalization** 

INEQ_1	INEQ_0	INPUT EQUALIZATION (dB)
0	0	3
0	1	5
1	0	7
1	1	9

**Table 2. Output Deemphasis/Preshoot** 

OEQ_2	OEQ_1	OEQ_0	OUTPUT DEEMPHASIS RATIO (dB)	PRESHOOT
0	0	0	01	No
0	0	1	3.51	No
0	1	0	61	No
0	1	1	62	No
1	0	0	3.51	Yes
1	0	1	6 <sup>1</sup>	Yes
1	1	0	93	Yes
1	1	1	91	Yes

<sup>&</sup>lt;sup>1</sup> Peak-to-peak swing is 1.0V.

**Table 3. Receiver Detection Input Function** 

RXDET	EN	DESCRIPTION
X	0 Receiver detection is inactive	
X	1	Following a rising edge of EN signal, indefinite retry until a receiver is detected for at least one channel. Retries stop a few times after any channel is detected.
Rising/Falling Edge	1	Initiate receiver detection

X = Don't care.

#### **Programmable Output Deemphasis**

Programmable output deemphasis/preshoot for channel A is controlled by the three bits: OEQA2, OEQA1, OEQA0 and channel B is controlled by the three bits: OEQB2, OEQB1, OEQB0 (Table 2.)

#### **Receiver Detection**

The device features receiver detection on each channel. Upon initial power-up, if EN is high, receiver detection initializes. Receiver detection can also be initiated on a rising or falling edge of the RXDET input when EN is high. During this time, the part remains in low-power standby mode and the outputs are squelched, despite the logichigh state of EN. Until a channel has detected a receiver, the receiver detection repeats indefinitely on each channel. If a channel detects a receiver, the other channel is limited to a few retries. Upon receiver detection, input common-mode termination and electrical idle detection are enabled (Table 3.)

#### **Electrical Idle Detection**

The device features electrical idle detection to prevent unwanted noise from being redriven at the output. When the device detects the differential input has fallen below the electrical idle low threshold, it squelches the output. For differential input signals that are above the electrical idle high threshold, the device turns on the output and redrives the signal. Electrical idle threshold is set independently for each channel. Drive the EIHAL, EILAL, and EIHAH for channel A and drive EIHBL. EILBL. and EIHBH for channel B as shown in Table 4 to set the electrical idle high and low threshold limits. There is little variation in output common-mode voltage between electrical idle and redrive modes.

Table 4. Electrical Idle Detection Limits Threshold Setting

EIL_L	EIH_H	EIH_L	THRESHOLD LOW LIMIT (typ) (mV)	THRESHOLD HIGH LIMIT (typ) (mV)
0	0	0	118	120
0	0	1	88	90
0	1	0	148	150
0	1	1	Not Valid	Not Valid
1	0	0	92	107
1	0	1	Not Valid	Not Valid
1	1	0	125	135
1	1	1	Not Valid	Not Valid

<sup>&</sup>lt;sup>2</sup> Peak-to-peak swing is 1.2V.

<sup>&</sup>lt;sup>3</sup> Peak-to-peak swing is 0.9V.

#### **Applications Information**

#### Layout

Circuit board layout and design can significantly affect the performance of the device. Use good high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on data signals. Power-supply decoupling capacitors must be placed as close as possible to V<sub>CC</sub>. Always connect V<sub>CC</sub> to a power plane. It is recommended to run receive and transmit on different layers to minimize crosstalk.

#### Exposed-Pad Package

The exposed-pad, 40-pin TQFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the device must be soldered to the circuit board ground plane for proper thermal performance. For more information on exposed-pad packages, refer to Maxim Application Note HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages.

#### **Power-Supply Sequencing**

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings could cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply GND then V<sub>CC</sub> before applying signals, especially if the signal is not current limited.

#### **Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE	
MAX14950ACTL+	0°C to +70°C	40 TQFN-EP*	

<sup>+</sup>Denotes a lead(Pb)-free/RoHS-compliant package.

#### **Chip Information**

PROCESS: BICMOS

#### **Package Information**

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE	PACKAGE	OUTLINE	LAND
TYPE	CODE	NO.	PATTERN NO.
40 TQFN-EP	T4055+2	21-0140	90-0002

<sup>\*</sup>EP = Exposed pad.

# **Single-Lane PCIe Equalizer/Redriver**

### **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	_

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